REMARKS

Request for an Examiner's Interview

The Applicants and the Applicant's attorney hereby request a telephone interview with the Examiner in order to expedite the prosecution of the present patent application. Applicants have also requested a telephone interview with the Examiner in the Amendment and Response for RCE filed on November 29, 2006.

Pending Claims:

Claims 1-11, 13-14 and 23-36 are currently pending in the present application. Claims 1, 3, 5, 13-14, 23, 34, and 36 have been amended. Claims 15-22 have been cancelled without prejudice. Upon entry of the present Amendment, reconsideration of claims 1-11, 13-14 and 23-36 in light of the amendments and remarks is respectfully requested.

Rejection Under 35 U.S.C. §112

The Applicants' Attorney acknowledge with appreciation that the rejections of claims 1-14 and 23-36 under 35 U.S.C. §112 have been withdrawn.

Rejections under 35 U.S.C. §102

Claims 1-5, 7-8, 10-11, 13-14, and 34-36 have been rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Publication No. 2001/0003187 to Aoki et al. (hereinafter "Aoki"). The Office Action dated February 27, 2007 states that Aoki teaches the invention as claimed in independent claims 1, 23, and 34.

To anticipate a claim under 35 U.S.C. §102, a single reference must teach every aspect of

the claimed invention either explicitly or impliedly. Any feature not directly taught by the reference must be inherently present in the reference. Thus, a claim is anticipated by a reference only if each and every element of the claim is described, either expressly or inherently, in a single prior art reference.

Independent claims 1 and 34 have been amended to more clearly define the invention. In particular, independent claim 1 has been amended to recite a method of compiling a high level language to map a plurality of tasks and a plurality of data onto a very long instruction word configurable multiple processor, distributed memory hardware architecture including the step of describing a task-level network of behaviors that defines an embedded system in the very long instruction word configurable multiple processor. Also, claim 1 has been amended to recite the step of allocating the plurality of tasks to at least two processors and allocating the plurality of data to at least two distributed memory in the very long instruction word configurable multiple processor, distributed memory hardware architecture in response to the predicted schedule of tasks. In addition, claim 1 has been amended to recite the step of generating machine executable code with the allocated plurality of tasks and allocated plurality of data for the very long instruction word configurable multiple processor, distributed memory hardware architecture that enables parallel execution of very long instruction word operations.

The Applicants submit that the prior art of record including Aoki does not describe allocating resources in a very long instruction word processor and does not describe generating machine executable code with the allocated plurality of tasks and allocated plurality of data for the very long instruction word configurable multiple processor that enables parallel execution of very long instruction word operations as claimed in independent claim 1. The present invention is at least in part the realization that a high level language can be compiled to map a plurality of

tasks and a plurality of data onto a very long instruction word configurable multiple processor as claimed in independent claim 1 as currently amended. Very long instruction word configurable multiple processor architectures have severe constraints on the use of multiple shared memories between very long instruction word slots for achieving high performance. In addition, very long instruction word configurable multiple processor architectures have severe constraints on parallelizing algorithms for achieving high performance.

In other words, methods of mapping a plurality of tasks and a plurality of data onto a very long instruction word configurable multiple processor, distributed memory hardware architecture are significantly different from similar methods known in the prior art for standard length and RISC instruction words. Similar prior art methods for configurable very long instruction word processor architectures are known for single processor architectures. These prior art methods typically require a relatively large amount of memory for proper operation. In these prior art methods, the ability to allocate a plurality of tasks is limited to allocating tasks in predefined locations in the data path. The advantage of using very long instruction word configurable multi-processor architectures is that the very long instruction word processors have multiple slots where each of the slots contain a unique set of processing elements. The processing elements in particular very long instruction word slot are overlaid and only one can be used at a time

Known configurable very long instruction word processor architectures are difficult to support with high-level language compilers and difficult to design with known compilers. These compilers are relatively complex. Configurability is typically achieved by custom assembly language programming. Using assembly language programming is more difficult and time consuming and, therefore increases the time-to-market and the cost of goods using such

processors.

Therefore, the Applicants submit that the methods described in Aoki can not be used with very long instruction word processor architectures as claimed in independent claim 1. Therefore, the Applicants submit that independent claim 1 is allowable and that dependent claims 1-11, 13-14 are allowable as depending upon an allowable base claim.

Similarly, independent claim 34 has been amended to recite a compiler for mapping a plurality of tasks and data onto a very long instruction word configurable multiple processor that includes means for allocating the plurality of tasks and data to at least two processors and to at least two distributed memories in a very long instruction word configurable multiple processor, distributed memory architecture, respectively, in response to a predicted schedule of tasks to enable parallel execution of very long instruction word operations.

The prior art of record including Aoki does not describe the claimed method using a very long instruction word configurable multiple processor. In addition, it should be understood that independent claim 34 is drafted in means plus function language under 35 U.S.C. §112 paragraph 6, which requires that the limitations be interpreted in light of the structure disclosed in the specification. Therefore, the Applicants submit that independent claim 34 is allowable and that dependent claims 35-36 are allowable as depending upon an allowable base claim.

Rejections under 35 U.S.C. §103(a)

Claims 6, 9 and 23-33 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Aoki in view of U.S. Patent No. 6,110,220 to Dave (hereinafter "Dave"). In light of the above arguments made in connection with the rejection under 35 U.S.C.

§102(e), the Applicants submit that independent claim 1 is allowable and that dependent claims 6-9, as currently amended, are allowable as depending upon an allowable base claim.

Regarding independent claim 23, this claim has been amended to recite a method of compiling a high level language to a schedule of tasks in a very long instruction word configurable multiple processor, distributed memory architecture including the step of generating machine executable code with an allocated task for the very long instruction word configurable multiple processor, distributed memory hardware architecture that enables parallel execution of very long instruction word operations.

In light of the above arguments made in connection with the rejection under 35 U.S.C. §102(e), the Applicants submit that the prior art of record including Aoki does not describe the claimed method using a very long instruction word configurable multiple processor. Therefore, the Applicants submit that independent claim 23 is allowable and that dependent claims 24-33 are allowable as depending upon an allowable base claim.

CONCLUSION

Claims 1-11, 13-14 and 23-36 are pending in the present application. Claims 1, 3, 5, 13-14, 23, 34, and 36 have been amended. The Applicants respectfully request reconsideration of the pending claims in light of the amendments and arguments presented in this Amendment and Response.

The Applicant's Attorney has requested a telephonic interview to expedite prosecution of the present patent application. The Applicant's Attorney welcomes the opportunity to discuss any outstanding issues, and to work with the Examiner toward placing the application in condition for allowance. Authorization to charge Attorney's charge card for proper fees is given

in the EFS-Web filing submission papers. However, if that authorization is insufficient, the Commissioner is hereby authorized to charge any proper fees to Attorney's Deposit Account No. 501211.

Respectfully submitted,

Date: August 24, 2007
Reg. No. 40,137

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